Abstract of the Disclosure

A geometric DAC architecture includes a series of substantially identical sub-DACs, each sub-DAC having n taps. The sub-DACs are fed from a bias-DAC having m = (total number of taps needed)/n taps. The output of each of the m taps is increased geometrically at a rate of k^n. The geometric DAC architecture control lines desirably require only (m + n) taps compared with (m x n) taps for the simpler more conventional approach. Further, the geometric DAC architecture requires less real estate than the simpler more conventional approach, is easy to expand because it is modular, and generates an output current that is always monotonic, regardless of errors in transistor sizes and PVT variations. The n tap control lines are coded by alternately inverting n control line inputs between sub-DACs such that any state transition associated with the geometric DAC occurs with only one bit change in each of the control lines.